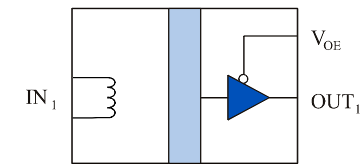
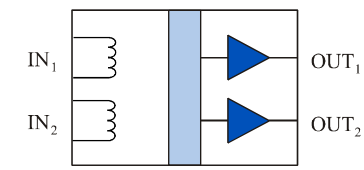
# IL600-Series Isolators

## Passive-Input Digital Isolators – CMOS Outputs

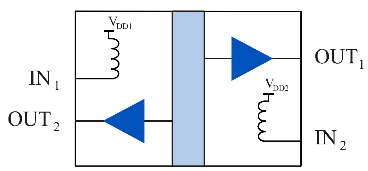
### Functional Diagrams



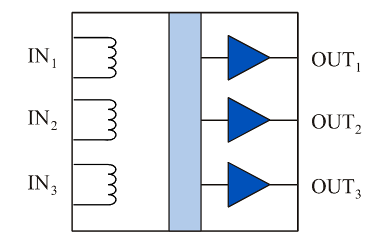
IL610



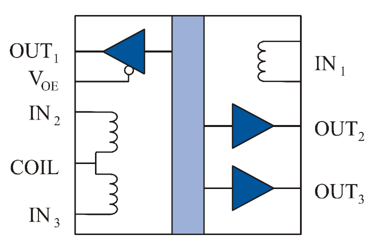
IL611



IL612



IL613



IL614

### Features

- Up to 100 Mbps data rate
- Flexible inputs with wide input voltage range
- 5 mA input current
- Deterministic default LOW and default HIGH versions
- No carriers or clocks for low EMI emissions and susceptibility
- 3 V to 5 V power supplies
- 44000 year barrier life
- –40°C to 85°C temperature range
- 2.5 kV isolation
- IEC 60747-17 (VDE 0884-17):2021-10; UL 1577
- 8-pin MSOP, SOIC, and PDIP packages
- 0.15", 0.3", or True 8™ mm SOIC packages

### Applications

- Optocoupler replacements
- Logic to control interfaces
- Differential line receivers
- Space-critical applications

### Description

The IL600 Series are passive input digital signal isolators with CMOS outputs. They have a similar interface but better performance and higher package density than optocouplers.

The devices are manufactured with NVE's patented* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology for small size, high speed, and low power.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

A resistor sets the input current; a capacitor in parallel with the current-limit resistor provides improved dynamic performance. Parts are available in both default HIGH output and default LOW versions.

These versatile components simplify inventory requirements by replacing a variety of optocouplers, functioning over a wide range of data rates, edge speeds, and power supply levels. The devices are available in various packages, as well as bare die.


*U.S. Patent number 5,831,426; 6,300,617 and others.

REV. AE

## Absolute Maximum Ratings[1]

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | –55[2] | | 150 | °C | |
| Junction Temperature | $T_J$ | –55 | | 150 | °C | |
| Ambient Operating Temperature | $T_A$ | –40[3] | | 85 | °C | |
| Supply Voltage | $V_{DD}$ | –0.5 | | 7 | V | |
| DC Input Current | $I_{IN}$ | –25 | | 25 | mA | |
| AC Input Current (Single-Ended Input) | $I_{IN}$ | –35 | | 35 | mA | |
| AC Input Current (Differential Input) | $I_{IN}$ | –75 | | 75 | mA | |
| Output Voltage | $V_O$ | –0.5 | | $V_{DD}$+1.5 | V | |
| Maximum Output Current | $I_O$ | –10 | | 10 | mA | |
| ESD (output enable CMOS inputs) | | | 2 | | kV | HBM |

## Recommended Operating Conditions

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | –40[3] | | 85 | °C | |
| Junction Temperature | $T_J$ | –40 | | 100 | °C | |
| Supply Voltage | $V_{DD}$ | 3.0 | | 5.5 | V | |
| Output Current | $I_{OUT}$ | –4 | | 4 | mA | |
| Common Mode Input Voltage | $V_{CM}$ | | | 400 | $V_{RMS}$ | |

**Note 1:** Operating at absolute maximum ratings will not damage the device. Parametric performance is not guaranteed at absolute maximum ratings.
**Note 2:** –55ºC applies to all except IL611-1E. -20ºC applies to IL611-1E
**Note 3:** –40ºC applies to all except IL611-1E. -20ºC applies to IL611-1E



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## Safety and Approvals

***IEC 60747-17 (VDE 0884-17):2021-10*** (Basic Isolation; VDE File Number 5016933-4880-0001):

- Isolation voltage ($V_{ISO}$): 2500 $V_{RMS}$
- Transient overvoltage ($V_{IOTM}$): 4000 $V_{PK}$
- Surge rating 4000 V
- Each part tested at 1590 $V_{PK}$ for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 $V_{PK}$ for 60 sec.; then 1358 $V_{PK}$ for 10 sec. with 5 pC partial discharge limit

- Working Voltage ($V_{IORM}$; pollution degree 2):

| Package | Part No. Suffix | Working Voltage |
|---|---|---|
| MSOP8 | -1 | 800 $V_{RMS}$ |
| SOIC8 | -3 | 700 $V_{RMS}$ |
| PDIP8 | -2 | 900 $V_{RMS}$ |
| Narrow-body SOIC16 | -3 | 700 $V_{RMS}$ |
| Wide-body SOIC16/True 8™ | None | 600 $V_{RMS}$ |

| Safety-Limiting Values | Symbol | Value | Units |
|---|---|---|---|
| Safety rating ambient temperature | $T_S$ | 180 | °C |
| Safety rating power (180°C) | $P_S$ | 270 | mW |
| Supply current safety rating (total of supplies) | $I_S$ | 54 | mA |

***UL 1577*** (Component Recognition Program File Number E207481)

- 2500 V rating for all types other than MSOP.
- Each part other than MSOP tested at 3000 $V_{RMS}$ (4240 $V_{PK}$) for 1 second; each lot sample tested at2500 $V_{RMS}$ (3530 $V_{PK}$) for 1 minute.
- MSOP rating 1000 V; tested at 1200 $V_{RMS}$ (1768 $V_{PK}$) for 1 second; each lot sample tested at 1500 $V_{RMS}$ (2121 $V_{PK}$) for 1 minute.

## Soldering Profile

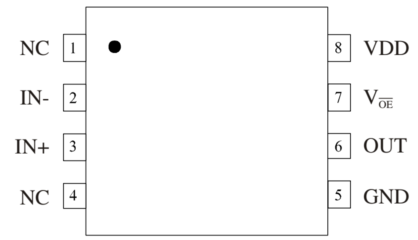
Per JEDEC J-STD-020C; MSL 1

## Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

## IL610/IL610F Pin Connections

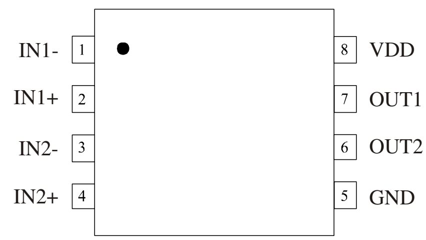
| | | |
|---|---|---|
| 1 | NC | No internal connection |
| 2 | IN– | Coil connection |
| 3 | IN+ | Coil connection |
| 4 | NC | No internal connection |
| 5 | GND | Ground return for $V_{DD}$ |
| 6 | OUT | Data out |
| 7 | $V_{\overline{OE}}$ | Output enable (internally held low with approx. 100 kΩ) |
| 8 | $V_{DD}$ | Supply Voltage |




IL610/IL610F

## IL611 Pin Connections

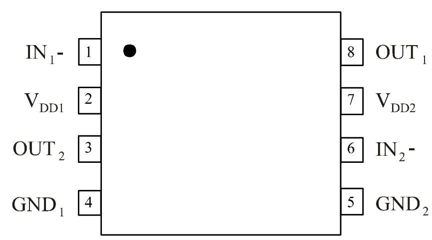
| | | |
|---|---|---|
| 1 | $IN_1$– | Channel 1 coil connection |
| 2 | $IN_1$+ | Channel 1 coil connection |
| 3 | $IN_2$– | Channel 2 coil connection |
| 4 | $IN_2$+ | Channel 2 coil connection |
| 5 | GND | Ground return for $V_{DD}$ |
| 6 | $OUT_2$ | Data out, channel 2 |
| 7 | $OUT_1$ | Data out, channel 1 |
| 8 | $V_{DD}$ | Supply Voltage |




IL611/IL611F

## IL612 Pin Connections

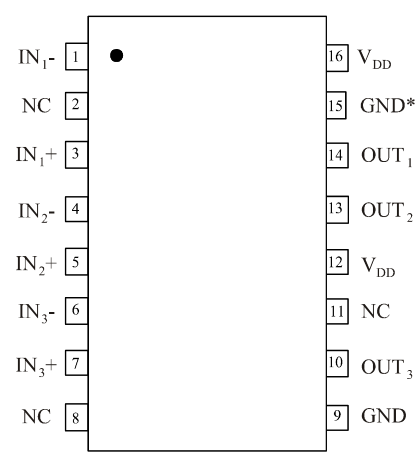
| | | |
|---|---|---|
| 1 | $IN_1$– | Channel 1 coil connection |
| 2 | $V_{DD1}$ | Supply Voltage 1 |
| 3 | $OUT_2$ | Data out, channel 2 |
| 4 | $GND_1$ | Ground return for $V_{DD1}$ |
| 5 | $GND_2$ | Ground return for $V_{DD2}$ |
| 6 | $IN_2$– | Channel 2 coil connection |
| 7 | $V_{DD2}$ | Supply Voltage 2 |
| 8 | $OUT_1$ | Data out, channel 1 |




IL612/IL612F

## IL613 Pin Connections

| | | |
|---|---|---|
| 1 | $IN_1$– | Channel 1 coil connection |
| 2 | NC | No connection (internally connected to pin 8) |
| 3 | $IN_1$+ | Channel 1 coil connection |
| 4 | $IN_2$– | Channel 2 coil connection |
| 5 | $IN_2$+ | Channel 2 coil connection |
| 6 | $IN_3$– | Channel 3 coil connection |
| 7 | $IN_3$+ | Channel 3 coil connection |
| 8 | NC | No connection (internally connected to pin 2) |
| 9 | GND | Ground return for $V_{DD}$ (internally connected to pin 15) |
| 10 | $OUT_3$ | Data out, channel 3 |
| 11 | NC | No connection |
| 12 | $V_{DD}$ | Supply Voltage. Pin 12 and pin 16 must be connected externally |
| 13 | $OUT_2$ | Data out, channel 2 |
| 14 | $OUT_1$ | Data out, channel 1 |
| 15 | GND | Ground return for $V_{DD}$ (internally connected to pin 9) |
| 16 | $V_{DD}$ | Supply Voltage. Pin 12 and pin 16 must be connected externally |

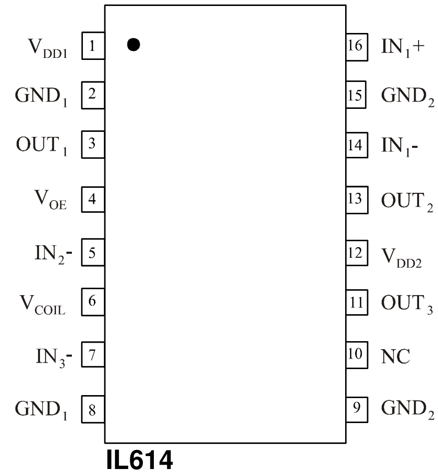



IL613/IL613F

Note: Pins 12 and 16 must be connected externally.

### IL614 Pin Connections

| | | |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage 1 |
| 2 | $GND_1$ | Ground return for $V_{DD1}$ (internally connected to pin 8) |
| 3 | $OUT_1$ | Data out, channel 1 |
| 4 | $V_{\overline{OE}}$ | Channel 1 data output enable. Internally held low with 100 kΩ |
| 5 | $IN_2–$ | Data in, channel 2 |
| 6 | $V_{coil}$ | Supply connection for channel 2 and channel 3 coils |
| 7 | $IN_3–$ | Data in, channel 3 |
| 8 | $GND_1$ | Ground return for $V_{DD1}$ (internally connected to pin 2) |
| 9 | $GND_2$ | Ground return for $V_{DD2}$ (internally connected to pin 15) |
| 10 | NC | No Connection |
| 11 | $OUT_3$ | Data out, channel 3 |
| 12 | $V_{DD2}$ | Supply Voltage 2 |
| 13 | $OUT_2$ | Data out, channel 2 |
| 14 | $IN_1–$ | Channel 1 coil connection |
| 15 | $GND_2$ | Ground return for $V_{DD2}$ (internally connected to pin 9) |
| 16 | $IN_1+$ | Channel 1 coil connection |



## Operating Specifications

| **Input Specifications** ($V_{DD}$ = 3 V − 5.5 V; T = −40°C – 85°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| Coil Input Resistance | $R_{COIL}$ | 47 | 85 | 112 | Ω | T = 25°C |
| | | 31 | 85 | 128 | Ω | T = −40°C – 85°C |
| Coil Resistance Temperature Coefficient | TC $R_{COIL}$ | | 0.2 | 0.25 | Ω/°C | |
| Coil Inductance | $L_{COIL}$ | | 9 | | nH | |
| DC Input Threshold (5 V) | $I_{INH-DC}$ | 0.5 | 3 | | mA | $V_{DD}$ = 4.5 V – 5.5 V |
| | $I_{INL-DC}$ | | 3.5 | 5 | mA | |
| DC Input Threshold (3 V) | $I_{INH-DC}$ | 0.3 | 0.5 | | mA | $V_{DD}$ = 3V – 3.6 V; no boost capacitor |
| | $I_{INL-DC}$ | | 5 | 8 | mA | |
| Dynamic Input Threshold (3 V) | $I_{INH-BOOST}$ | 0.5 | 3 | | mA | $V_{DD}$ = 3V – 3.6 V; $t_{IR} = t_{IF}$ = 3 ns; $C_{BOOST}$ = 16 pF |
| | $I_{INL-BOOST}$ | | 3.5 | 5 | mA | |
| Differential Input Threshold | $I_{INH-DIFF}$ | 0.5 | 3 | | mA | $V_{DD}$ = 3V – 5.5 V; input current reverses; boost cap not required |
| | $I_{INL-DIFF}$ | | 3.5 | 5 | mA | |
| Input Threshold Hysteresis | $I_{INH} - I_{INL}$ | | 1 | | mA | |
| Failsafe Input Current[(1)] (5 V) | $I_{INL-FS}$ | –25 | | 0.5 | mA | $V_{DD}$ = 4.5 V – 5.5 V |
| Failsafe Input Current[(1)] (3 V) | $I_{INH-FS}$ | –25 | | 0.3 | mA | $V_{DD}$ = 3 V – 3.6 V |
| | $I_{INL-FS}$ | 8 | | 25 | mA | |
| $V_{OE}$ Logic High Input Voltage | $V_{IH}$ | 2.4 | | $V_{DD}$ | V | |
| $V_{OE}$ Logic Low Input Voltage | $V_{IL}$ | 0 | | 0.8 | V | |
| Input Signal Rise and Fall Times | $t_{IR}$, $t_{IF}$ | | | 1 | µs | |
| Common Mode Transient Immunity | $\|CM_H\|,\|CM_L\|$ | | 100 | | kV/µs | |

**Notes:**

1. "Failsafe Operation" is defined as the input current required to guarantee an output state on power-up.
To guarantee failsafe input energization, the DC current supplied to the coil must be at least 8 mA using 3.3 V supplies versus 5 mA for 4.5 V or higher supplies.

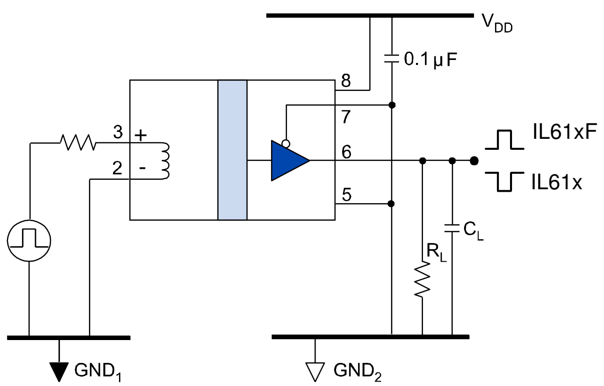



**Figure 1. Test circuit.**

| **5 V Electrical Specifications** ($V_{DD}$ = 4.5 V − 5.5 V; T = −40°C[(5)] – 85°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| Quiescent Supply Current | | | | | | |
| IL610 | $I_{DD}$ | | 2 | 3 | mA | $V_{DD}$ = 5 V, $I_{IN}$ = 0 |
| IL611 | $I_{DD}$ | | 4 | 6 | | |
| IL612 | $I_{DD1}$ | | 2 | 3 | | |
| IL612 | $I_{DD2}$ | | 2 | 3 | | |
| IL613 | $I_{DD}$ | | 6 | 9 | | |
| IL614 | $I_{DD1}$ | | 2 | 3 | | |
| IL614 | $I_{DD2}$ | | 4 | 6 | | |
| Logic High Output Voltage | $V_{OH}$ | 4.9 | 5 | | V | $V_{DD}$ = 5 V, $I_O$ = 20 µA |
| | | 4.0 | 4.8 | | V | $V_{DD}$ = 5 V, $I_O$ = 4 mA |
| Logic Low Output Voltage | $V_{OL}$ | | 0 | 0.1 | V | $V_{DD}$ = 5 V, $I_O$ = −20 µA |
| | | | 0.2 | 0.8 | V | $V_{DD}$ = 5 V, $I_O$ = −4 mA |
| Logic Output Drive Current | $\|I_O\|$ | 7 | 10 | | mA | |

| **5 V Switching Specifications** ($V_{DD}$ = 4.5 V − 5.5 V; T = −40°C[(5)] – 85°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| Data Rate | | 100 | | | Mbps | $t_{IR} = t_{IF}$ = 3 ns; $C_{BOOST}$ = 16 pF |
| Minimum Pulse Width[(1)] | PW | 10 | | | ns | |
| Propagation Delay | $t_{PHL}$; $t_{PLH}$ | | 8 | 15 | ns | |
| Average Propagation Delay Drift | $t_{PLH}$ | | 10 | | ps/°C | |
| Pulse Width Distortion $\|t_{PHL}-t_{PLH}\|$[(2)] | PWD | | 3 | 5 | ns | |
| Pulse Jitter[(3)] | $t_J$ | | | 100 | ps | |
| Propagation Delay Skew[(4)] | $t_{PSK}$ | −2 | | 2 | ns | |
| Output Rise / Fall Time (10–90%) | $t_R$; $t_F$ | | 2 | 4 | ns | |

**Notes:**

1. Minimum Pulse Width is the shortest pulse width at which the specified PWD is guaranteed.
2. PWD is defined as $\| t_{PHL} - t_{PLH} \|$.
3. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.
4. $t_{PSK}$ is equal to the magnitude of the worst case difference in $t_{PHL}$ and/or $t_{PLH}$ that will be seen between units at 25°C.
5. −20ºC for IL611-1E.

| **3.3 V Electrical Specifications** ($V_{DD}$ = 3 V − 3.6 V; T = −40°C[4] – 85°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| Quiescent Supply Current | | | | | | |
| IL610 | $I_{DD}$ | | 1.3 | 2 | mA | $V_{DD}$ = 3.3 V, $I_{IN}$ = 0 |
| IL611 | $I_{DD}$ | | 2.6 | 4 | | |
| IL612 | $I_{DD1}$ | | 1.3 | 2 | | |
| IL612 | $I_{DD2}$ | | 1.3 | 2 | | |
| IL613 | $I_{DD}$ | | 4 | 6 | | |
| IL614 | $I_{DD1}$ | | 1.3 | 2 | | |
| IL614 | $I_{DD2}$ | | 2.6 | 4 | | |
| Logic High Output Voltage | $V_{OH}$ | 3.2 | 3.3 | | V | $V_{DD}$ = 3.3 V, $I_O$ = 20 µA |
| | | 3.0 | 3.1 | | V | $V_{DD}$ = 3.3 V, $I_O$ = 4 mA |
| Logic Low Output Voltage | $V_{OL}$ | | 0 | 0.1 | V | $V_{DD}$ = 3.3 V, $I_O$ = −20 µA |
| | | | 0.2 | 0.8 | V | $V_{DD}$ = 3.3 V, $I_O$ = −4 mA |
| Logic Output Drive Current | $\|I_O\|$ | 7 | 10 | | mA | |

| **3.3 V Switching Specifications** ($V_{DD}$ = 3 V − 3.6 V; T = −40°C[4] – 85°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| Data Rate | | 100 | | | Mbps | $t_{IR}$ = $t_{IF}$ = 3 ns; $C_{BOOST}$ = 16 pF |
| Minimum Pulse Width[1] | PW | 10 | | | ns | |
| Propagation Delay Input to Output (High to Low) | $t_{PHL}$ | | 12 | 18 | ns | |
| Propagation Delay Input to Output (Low to High) | $t_{PLH}$ | | 12 | 18 | ns | |
| Average Propagation Delay Drift | $t_{PLH}$ | | 10 | | ps/°C | |
| Pulse Width Distortion $\|t_{PHL}-t_{PLH}\|$ [2] | PWD | | 3 | 5 | ns | |
| Propagation Delay Skew[3] | $t_{PSK}$ | −2 | | 2 | ns | |
| Output Rise Time (10–90%) | $t_R$ | | 3 | 5 | ns | |
| Output Fall Time (10–90%) | $t_F$ | | 3 | 5 | ns | |

**Notes:**

1. The Minimum Pulse Width is the shortest pulse width at which the specified PWD is guaranteed.
2. PWD is defined as $\| t_{PHL} - t_{PLH} \|$.
3. $t_{PSK}$ is equal to the magnitude of the worst-case difference in $t_{PHL}$ and/or $t_{PLH}$ that will be seen between units at 25°C.
4. -20ºC for IL611-1E

## Insulation Specifications

| Parameters | | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| Creepage Distance (external) | | | | | | | |
| MSOP | | | 3.01 | | | mm | |
| 0.15" SOIC | | | 4.03 | | | mm | |
| 0.3" SOIC | | | 8.03 | 8.3 | | mm | Per IEC 60601 |
| PDIP | | | 7.08 | | | mm | |
| Total Barrier Thickness (internal) | | | 0.012 | 0.013 | | mm | |
| Leakage Current | | | | 0.2 | | μA | 240 $V_{RMS}$, 60 Hz |
| Barrier Resistance | | $R_{IO}$ | | $>10^{14}$ | | | 500 V |
| Barrier Capacitance | | $C_{IO}$ | | 7 | | Ω ǁ pF | f = 1 MHz |
| Comparative Tracking Index | | CTI | ≥175 | | | V | Per IEC 60112 |
| High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life) | AC | $V_{IO}$ | 1000 | | | $V_{RMS}$ | At maximum operating temperature |
| | DC | | 1500 | | | $V_{DC}$ | |
| Barrier Life | | | | 44000 | | Years | 100°C, 1000 $V_{RMS}$, 60% CL activation energy |

## Thermal Characteristics

| Parameter | | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| Junction–Ambient Thermal Resistance | MSOP8<br>0.15" SOIC8<br>0.15" SOIC16<br>0.3" SOIC16<br>PDIP8 | $\theta_{JA}$ | | 184<br>134<br>82<br>67<br>114 | | °C/W | Double-sided PCB in free air |
| Junction–Case (Top) Thermal Resistance | MSOP8<br>0.15" SOIC8<br>0.15" SOIC16<br>0.3" SOIC16<br>PDIP8 | $\theta_{JC}$ | | 15<br>10<br>8<br>12<br>36 | | °C/W | Double-sided PCB in free air |
| Junction–Ambient Thermal Resistance | 0.3" SOIC | $\theta_{JA}$ | | 46 | | °C/W | 2s2p PCB in free air per JESD51 |
| Junction–Case (Top) Thermal Resistance | 0.3" SOIC | $\theta_{JC}$ | | 9 | | °C/W | 2s2p PCB in free air per JESD51 |
| Power Dissipation | MSOP8<br>0.15" SOIC8<br>0.15" SOIC16<br>0.3" SOIC16<br>PDIP8 | $P_D$ | | | 500<br>675<br>675<br>1500<br>800 | mW | |

## Typical Performance Graphs

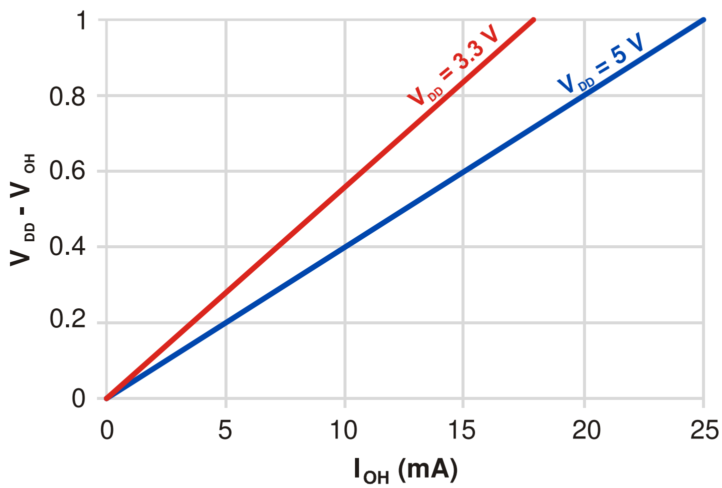



**Figure 2. Typical high output voltage vs. load.**

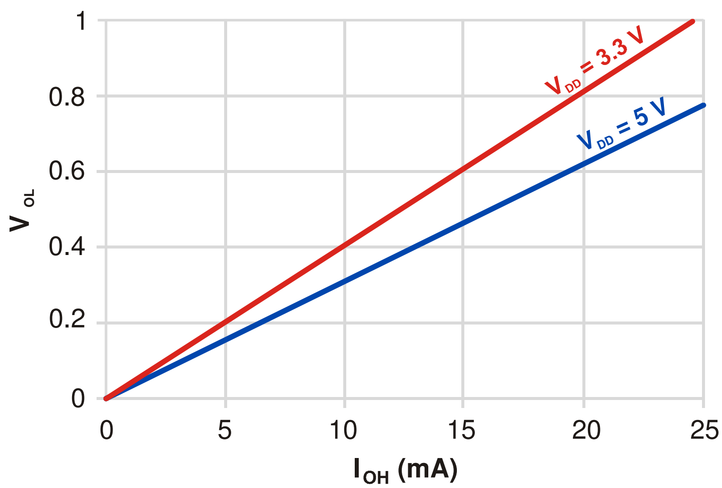



**Figure 3. Typical low output voltage vs. load**

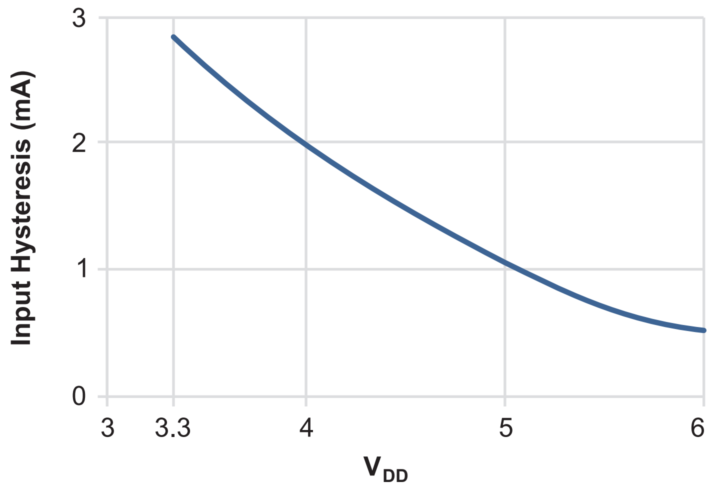



**Figure 4. Typical input threshold current hysteresis.**

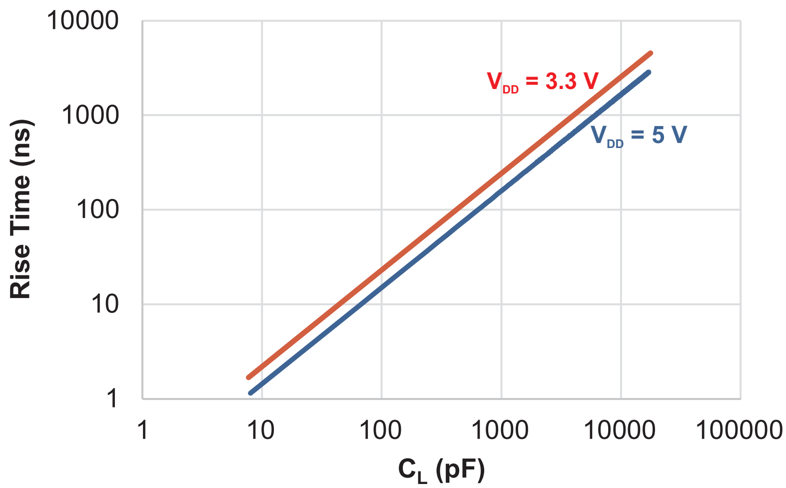



**Figure 5. Typical output rise time vs. load capacitance**

## Applications Information

### Overview

Figure 7 shows the IL600-Series block diagram. The coil, GMR, and support integrated circuitry are integrated on a single chip:

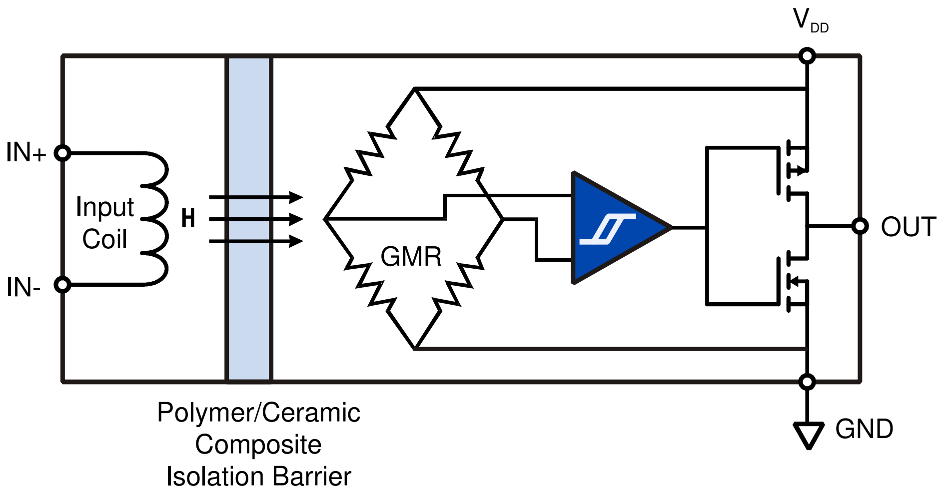



**Figure 6. IL61x block diagram (each channel).**

### Input Coil

IL600-Series Isolators' current-mode architecture avoids semiconductor structures on the inputs and input-side power supplies, providing unique flexibility. Changes in current flow into the input coil result in logic state changes at the output. Input-stage hysteresis improves noise immunity.

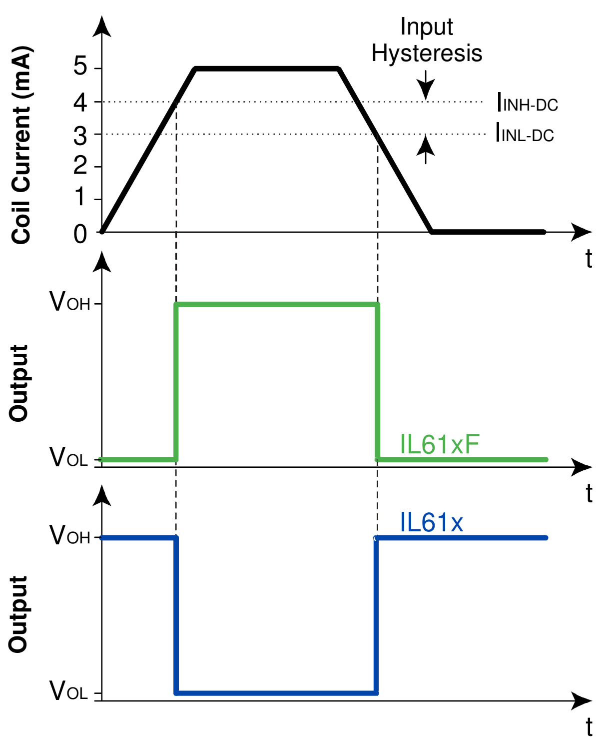



**Figure 7. Typical IL61x and IL61xF transfer functions.**

### GMR Wheatstone Bridge

The heart of the Isolators is a Wheatstone bridge constructed of GMR resistor elements. The current in the coil driven from the input side of the isolator creates a magnetic field that switches the GMR in the bridge. Thus the signal is transmitted by magnetic field.

### Schmitt Trigger and Output Stage

The change in the bridge is detected by a Schmitt trigger comparator. This drives a push-pull MOSFET output stage. The outputs have deterministic defaults when the input coil is unenergized (LOW for the IL61xF and HIGH for the IL61x).

### Coil Polarity

Current from (In+) to (In−) energizes the coil and switches the output from its default state. Zero or negative current will cause the output to switch to the default state. The coil input is analogous to the LED in an optocoupler, with (In+) analogous to the LED anode, and (In−) analogous to the cathode.

### Input Resistor Selection

A resistor sets the coil input current:

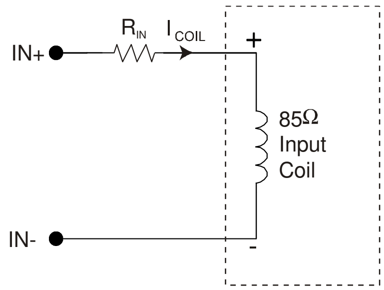



**Figure 8. Input resistor.**

The input resistor can be on either side of the coil, although it is shown of the (+) input in most of our circuits. There is no limit to input voltages because there are no semiconductor input structures.

Worst-case logic low threshold current is 8 mA, which is for single-ended operation with a 3 V supply. In differential mode, where the input current reverses, the logic low threshold current is 5 mA for the range of supplies. A "boost capacitor" creates current reversals at edge transitions, reducing the input logic low threshold current to the differential level of 5 mA.

### Typical Resistor Values

The following table shows typical values for the external resistor for 5 mA coil current. The values are approximate and should be adjusted for temperature or other application specifics:

| $V_{COIL}$ | Coil Resistor |
|---|---|
| 3.3 V | 510 Ω |
| 5 V | 820 Ω |

### Maximum Coil Current

Absolute Maximum unipolar coil current is 25 mA, while bipolar drive allows up to ±75 mA. The difference in specifications is due to the risk of electromigration of coil metals under constant current flow. Long-term unipolar DC current flow above 25 mA can cause erosion of the coil metal. In differential mode, erosion takes place in both directions as each current cycle reverses and has no net effect up to the absolute maximum current.

An advantage over optocouplers and other high-speed couplers in differential mode is that no reverse bias protection for the input structure is required for a differential signal.

***Boost Capacitor***
A "boost capacitor" in parallel with the current-limiting resistor boosts the instantaneous coil current at the signal transition. This ensures switching and reduces propagation delay and reduces pulse-width distortion. The optimal value of the boost capacitor is based on the rise and fall times of the signal driving the inputs. The instantaneous boost capacitor current is proportional to input edge speeds ($C\frac{dV}{dt}$). Select a capacitor value based on the rise and fall times of the input signal to be isolated that provides approximately 20 mA of additional "boost" current. Figure 12 is a guide to boost capacitor selection. For high-speed logic signals ($t_r$,$t_f$ < 10 ns), a 16 pF capacitor is recommended. The capacitor value is generally not critical; if in doubt, choose a higher value:

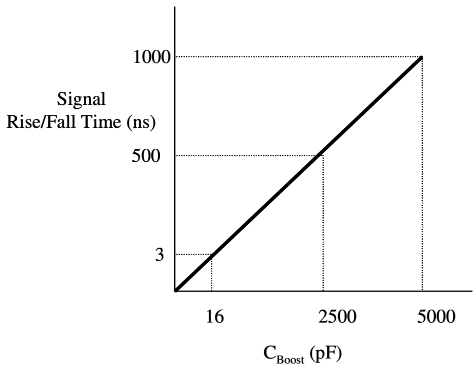



**Figure 9. $C_{boost}$ selection.**

**Drive Configurations**
As the figures below show, IL600-Series Isolators can be configured with the input referenced to ground, referenced to a logic supply, or in a bipolar configuration.

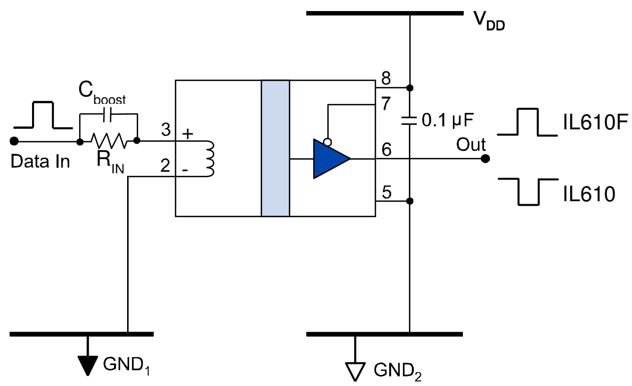



**Figure 10. Input referenced to ground.**

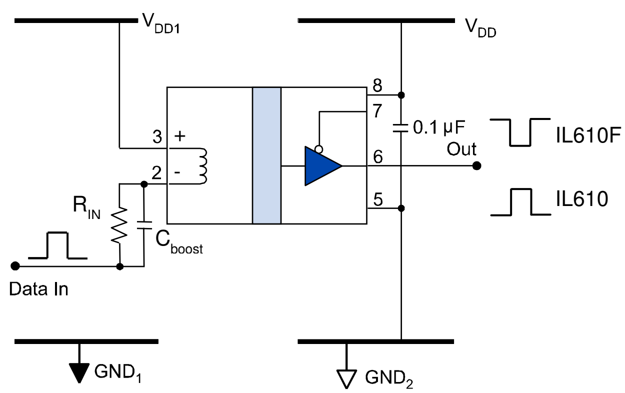



**Figure 11. Input referenced to logic supply.**

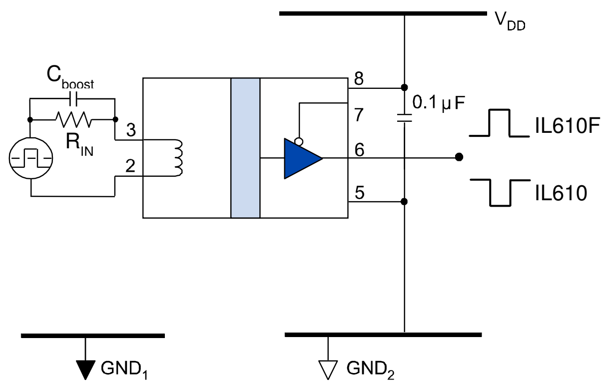



**Figure 12. Bipolar drive.**

### Single-Ended or Differential Input

The IL610, IL611, IL613, and channel 1 of the IL614 can be run with single-ended or differential inputs. In the differential mode, current will naturally flow through the coil in both directions without a boost capacitor, although the capacitor can still be used for increased external field immunity or improved pulse-width distortion. Bipolar drive increases the absolute maximum coil current, minimizes the required input current with a 3.3-volt supply, and maximizes immunity to external magnetic fields. No reverse bias protection for the input structure is required for a bipolar signal.

### Power Supply Decoupling

0.1 μF decoupling capacitors are recommended for the power supplies ($V_{DD}$, $V_{DD1}$, and $V_{DD2}$). The capacitors should be as close as possible to the $V_{DD}$ pins.

### Maintaining Creepage

Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

### Electromagnetic Compatibility and Magnetic Field Immunity

IL600-Series isolators are ideal for harsh industrial environments with low emitted fields and very high external magnetic field immunity. Because IL600-Series Isolators are completely static, they do no emitted any EMI.

### Internal Shielding and Inherent Common-Mode Field Immunity

IsoLoop Isolators operate by imposing a magnetic field on a GMR sensor, which translates the change in field into a change in logic state. A magnetic shield and a Wheatstone Bridge configuration provide superb immunity to external magnetic fields.

***Inherent AC magnetic field immunity***

Unlike inductive or capacitive which transmit and detect high-frequency carriers, IsoLoop Isolators do not rely on AC signals, and are inherently insensitive to AC magnetic fields. It is harder to disrupt an isolated AC signal with an external magnetic field than a DC signal. This enhances the magnetic immunity in switch-mode power control applications. Immunity to external magnetic fields can be enhanced by (1) optimal orientation of the device with respect to the field direction and (2) the use of bipolar coil inputs.

1. *Orientation of the device with respect to the external field*

   An applied field in the "H1" direction is the worst case for magnetic immunity. In this case, the external field is in the same direction as fields generated on-chip. An applied field in direction "H2" has considerably less effect and results in higher magnetic immunity.

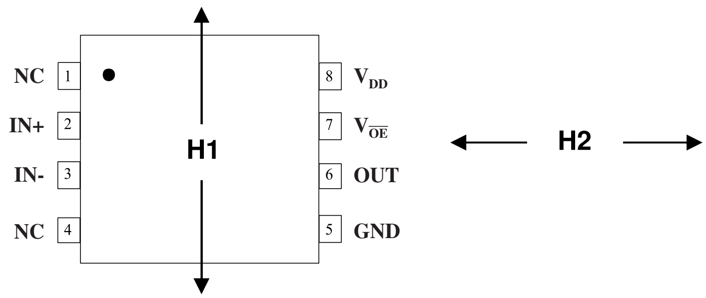



**Figure 13. Orientation with respect to the external field.**

2. *Bipolar coil input*

   Regardless of orientation, a bipolar input on the coil improves magnetic immunity. The higher the coil current, the higher the on-chip fields, and the higher the immunity to external fields.

| Method | Approx. Immunity | Immunity Description |
|---|---|---|
| Field applied in H1 direction | ±2 mT | A DC current of 100 A flowing in a conductor 1 cm from the device could cause disturbance. |
| Field applied in H2 direction | ±7 mT | A DC current of 140 A flowing in a conductor 1 cm from the device could cause disturbance. |
| Field applied in any direction but with a bipolar input to the coil | ±25 mT | A DC current of 1250 A flowing in a conductor 1 cm from the device could cause disturbance. |

## Illustrative Applications

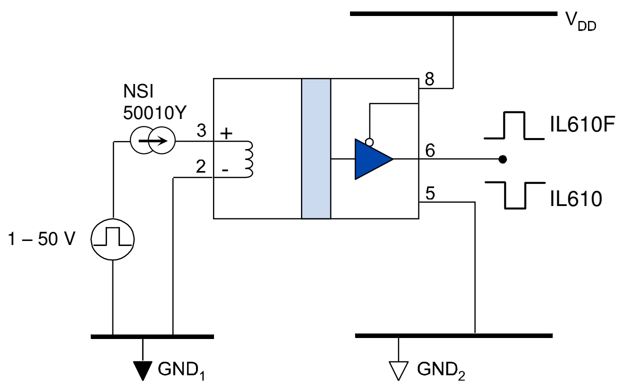



**Figure 14. Wide input voltage range using a current regulator.**

A self-biasing transistor current regulator can be used instead of an input resistor in series with the coil to provide a wide range of input voltages without overdriving or under driving the coil.

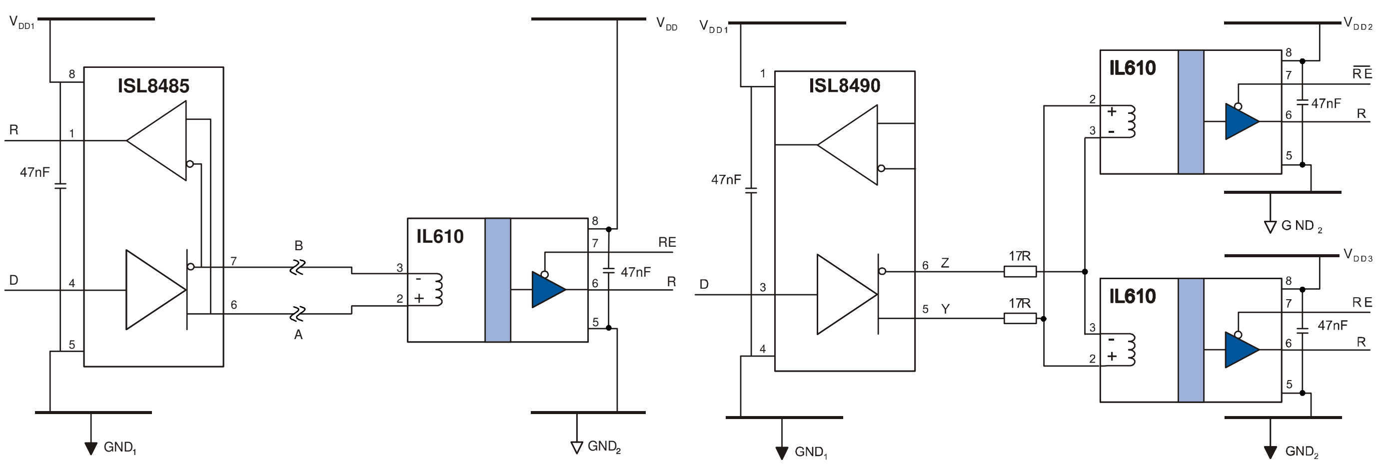



**Figure 15. Isolated RS-485 and RS-422 Receivers Using IL610s.**

IL610 components can be used as simple isolated RS-485 or RS-422 receivers, terminating signals at the IL610 for a fraction of the cost of an isolated node. Cabling is simplified by eliminating the need to power the input side of the receiving board. No current-limiting resistor is needed for a single receiver because it will draw less current than the driver maximum. Current limiting resistors allow at least eight nodes without exceeding the maximum load of the transceiver. Placement of the current-limiting resistors on both lines provides better dynamic signal balance. There is generally no need for line termination resistors below data rates of approximately 10 Mbps because the IL610 coil resistance of approximately 85 Ω is close to the characteristic impedance of most cables. The circuit is intrinsically open-circuit failsafe because the IL610 is guaranteed to switch to the high state when the coil input current is less than 0.5 mA.

| Number of Nodes | Current Limit Resistors (Ω) |
|---|---|
| 1 | None |
| 2 | 17 |
| 3 | 22 |
| 4 | 27 |
| 5 | 27 |
| 6 | 27 |
| 7 | 30 |
| 8 | 33 |

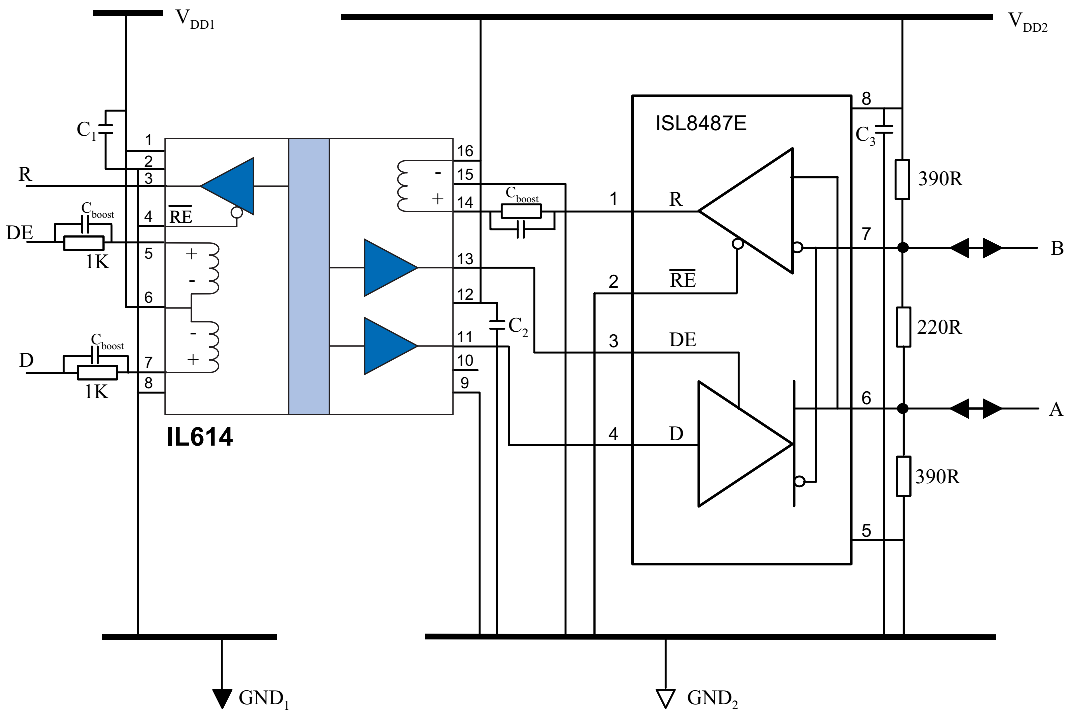



**Figure 16. Isolated RS-485 – Fractional Load.**

The unique IL614 three-channel isolator can be used as part of a multi-chip design with a variety of non-isolated transceivers. The IL614 provides 2.5 $kV_{RMS}$ isolation (1 minute) and 100 kV/μs transient immunity. The IL614-3 is in a narrow-body (0.15 inch-wide) package when board space is critical.

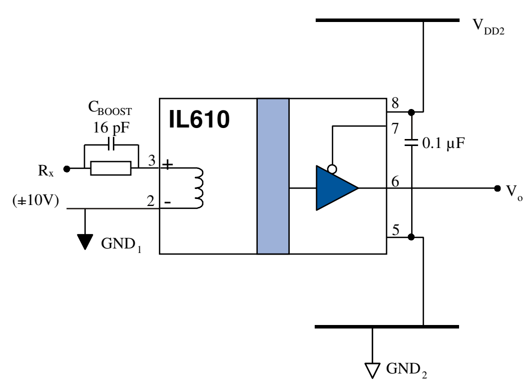



**Figure 17. Isolated RS-232 Receiver Using IL610.**

An IL610 can be used as a simple isolated RS-232 receiver. Most RS-232 nodes have at least 5 mA drive capability to switch the IL610. Cabling is simplified by eliminating the need to power the input side of the receiving board. A similar circuit can be used for RS-422/RS-485, LVDS, or other differential networks. The IL610-1 is a unique MSOP isolator when board space is critical.



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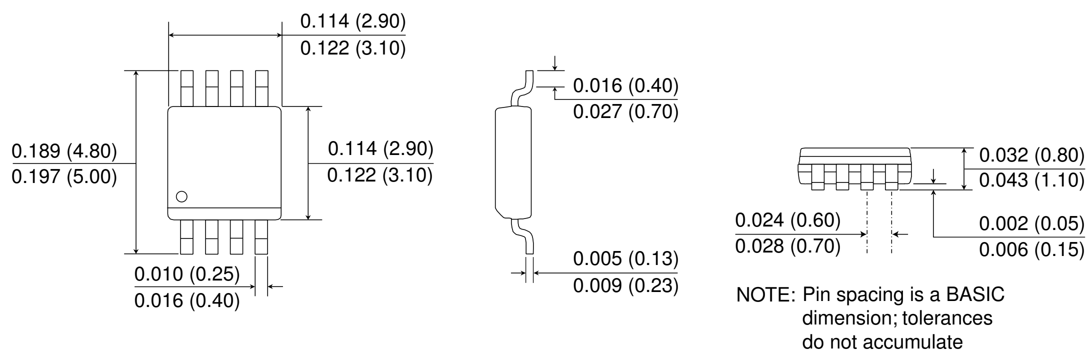
## Package Drawings

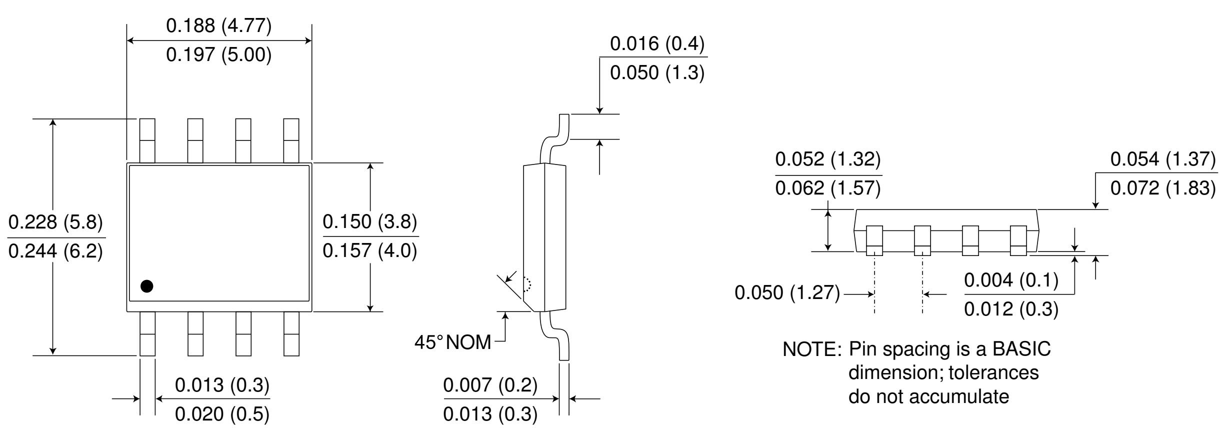
### **8-pin MSOP** (-1 suffix)

Dimensions in inches (mm); scale = approx. 5X



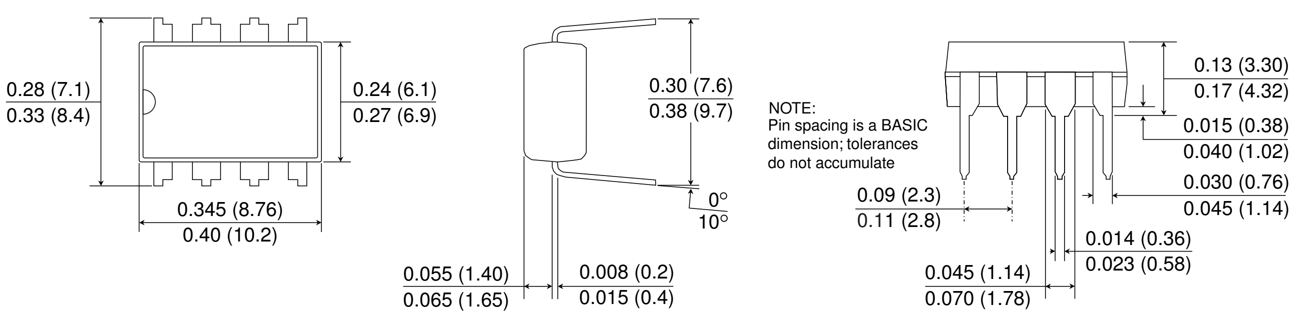

### **8-pin SOIC Package** (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X

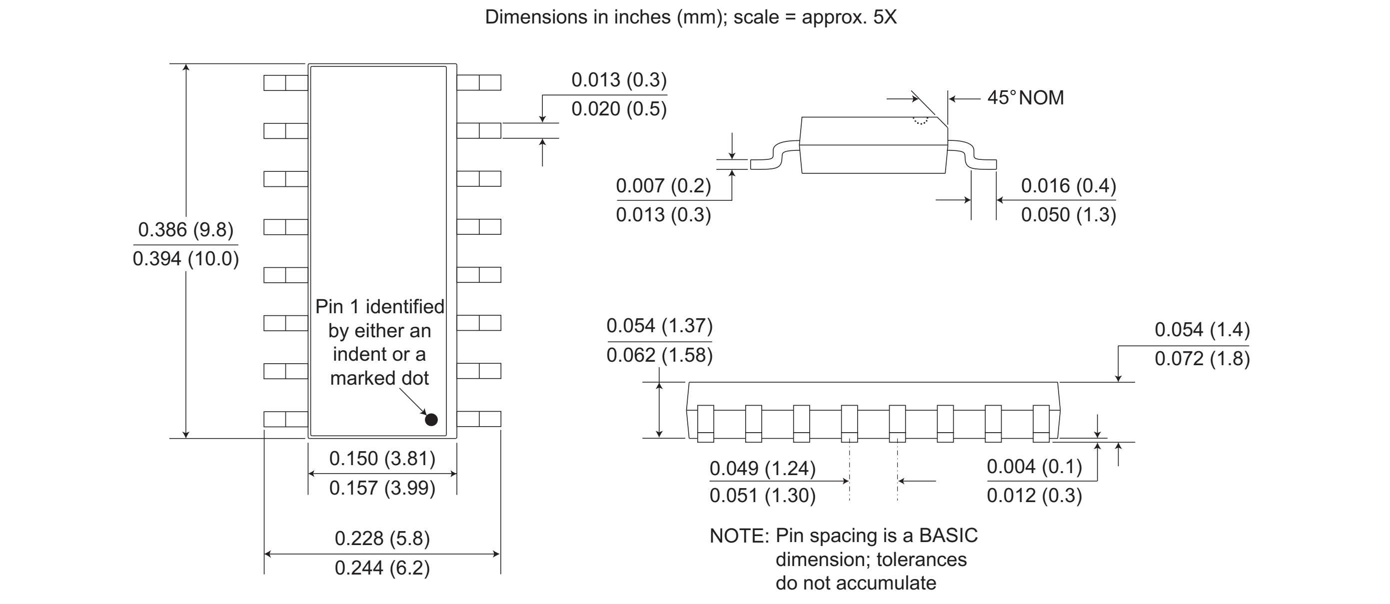



### **8-pin PDIP** (-2 suffix)

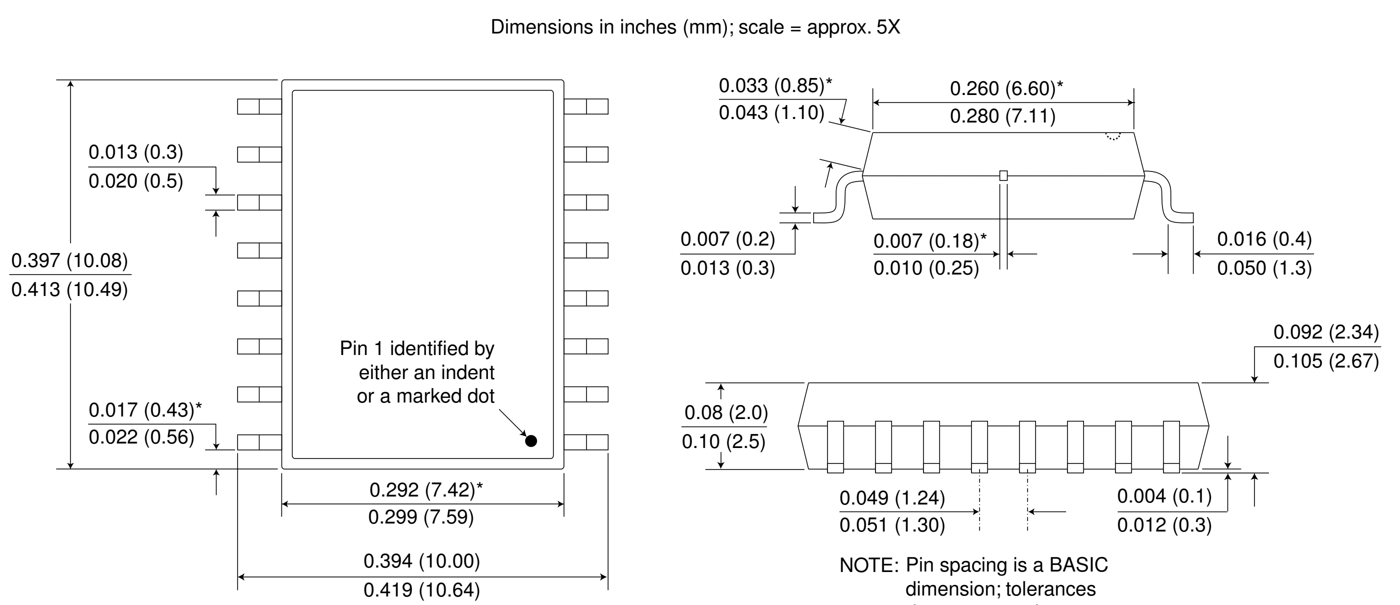
Dimensions in inches (mm); scale = approx. 2.5X



## 0.15" 16-pin SOIC Package (-3 suffix)




## 0.3" 16-pin SOIC Package (no suffix)




*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

## Ordering Information and Valid Part Numbers

# IL 6xx F - 1 E TR13

**Bulk Packaging**
- Blank = Tube
- TR7 = 7" Tape and Reel
- TR13 = 13" Tape and Reel

**Package**
- E = RoHS Compliant

**Package Type**
- Blank = 0.3" SOIC
- -1 = MSOP
- -2 = PDIP
- -3 = 0.15" SOIC
- -5 = Bare die

**Default Output**
- Blank = HIGH
- F = LOW

**Base Part Number**
- 610 = Single Channel
- 611 = 2 Drive Channels
- 612 = 1 Drive Channel, 1 Receive Channel
- 613 = 3 Drive Channels
- 614 = 2 Drive Channels, 1 Receive Channel

**Product Family**
- IL = Isolators

**IL610 Valid Part Numbers**
IL610-1E
IL610F-1E
IL610-2E
IL610-3E
IL610-5

**IL611 Valid Part Numbers**
IL611-1E
IL611F-1E
IL611-2E
IL611-3E

**IL612 Valid Part Numbers**
IL612-2E
IL612-3E

**IL613 Valid Part Numbers**
IL613E
IL613-3E

**IL614 Valid Part Numbers**
IL614E
IL614-3E

RoHS
COMPLIANT

## Revision History

**ISB-DS-001-IL600-AE**
**October 2025**

**Changes**
- Added IL610F-1E and IL611F-1E default-LOW versions.
- Reversed coil polarity labeling for applicability to default-HIGH and default-LOW versions.
- Increased Common Mode Transient Immunity specification from 20 to 100 kV/µs (p. 6).
- Added Typical Performance Graphs (p. 10).
- Changed magnetic immunity units from G to mT (SI units); clarified “Immunity Descriptions” (p. 13).
- Added SBT current-limiter application diagram (p. 17).
- Changed channel-direction terminology from “Drive” to “Transmit” (p. 21).
- Misc. cosmetic changes.

**ISB-DS-001-IL600-AD**
**October 2022**

**Changes**
- Upgrade to VDE 0884-17 (p. 3).
- Increased Working Voltage ratings based on latest VDE testing (p. 3).
- Added $V_{OE}$ logic high and low input voltage specifications (p. 6).
- Added thermal characteristics (p. 9).

**ISB-DS-001-IL600-AC**

**Changes**
- Corrected 8-pin SOIC package outline dimensions.
- Changed low temperature specification for IL611-1E to −20°C.

**ISB-DS-001-IL600-AB**

**Changes**
- IEC 60747-5-5 (VDE 0884) certification.
- Upgraded from MSL 2 to MSL 1.
- Rearranged input threshold specifications so maximum is more than minimum.

**ISB-DS-001-IL600-AA**

**Changes**
- Added VDE 0884 pending.
- Updated package drawings.
- Added recommended solder pad layouts.
- Clarified circuit polarities.

**ISB-DS-001-IL600-Z**

**Changes**
- Detailed isolation and barrier specifications.
- Cosmetic changes.

**ISB-DS-001-IL600-Y**

**Changes**
- Clarified Test Circuit 2 differential operation diagram (p.5).

**ISB-DS-001-IL600-X**

**Changes**
- Separated and clarified Input Specifications.
- Added minimum/maximum coil resistance specifications.
- Merged and simplified “Operation” and “Applications” sections.

**ISB-DS-001-IL600-W**

**Changes**
- Update terms and conditions.

**ISB-DS-001-IL600-V**

**Changes**
- Additional changes to pin spacing specification on MSOP drawing.

**ISB-DS-001-IL600-U**

**Changes**
- Changed pin spacing specification on MSOP drawing.



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*October 2025*